ABSTRACT OF THE DISCLOSURE

An adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)* is disclosed. The adder comprises a bypass input *(bypass)* and a logic circuit, communicatively coupled to the bypass input *(bypass)*, the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input *(bypass)*.

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